Lecture-19

di / dt and dv / dt protection

3.10 \( \frac{dv}{dt} \) PROTECTION

The \( \frac{dv}{dt} \) across the thyristor is limited by using snubber circuit as shown in figure (a) below. If switch \( S_1 \) is closed at \( t = 0 \), the rate of rise of voltage across the thyristor is limited by the capacitor \( C_s \). When thyristor \( T_1 \) is turned on, the discharge current of the capacitor is limited by the resistor \( R_s \) as shown in figure (b) below.

![Fig.3.18 (a)](image1)

![Fig.3.18 (b)](image2)

![Fig.3.18 (c)](image3)
The voltage across the thyristor will rise exponentially as shown by fig (c) above. From fig (b) above, circuit we have (for SCR off)

\[ V_s = i \cdot t \cdot R_s + \frac{1}{C} \int i \cdot t \cdot dt + V_c \quad 0 \quad \text{for } t = 0. \]

Therefore \[ i \cdot t = \frac{V_s}{R_s} e^{-\frac{t}{\tau_s}}, \text{ where } \tau_s = R_s C_s \]

Also \[ V_T \cdot t = V_s - i \cdot t \cdot R_s \]

\[ V_T \cdot t = V_s - \frac{V_s}{R_s} e^{-\frac{t}{\tau_s}} \]

Therefore \[ V_T \cdot t = V_s - V_s e^{-\frac{t}{\tau_s}} = V_s \left[ 1 - e^{-\frac{t}{\tau_s}} \right] \]

At \( t = 0 \), \[ V_T \cdot 0 = 0 \]

At \( t = \tau_s \), \[ V_T \cdot \tau_s = 0.632 V_s \]

Therefore \[ \frac{dv}{dt} = V_T \cdot \tau_s - V_T \cdot 0 \quad \tau_s \quad \frac{0.632 V_s}{R_s C_s} \]

And \[ R_s = \frac{V_s}{I_{rd}} \]

\( I_{rd} \) is the discharge current of the capacitor.

It is possible to use more than one resistor for \( \frac{dv}{dt} \) and discharging as shown in the figure (d) below. The \( \frac{dv}{dt} \) is limited by \( R_1 \) and \( C_s \). \( R_1 + R_2 \) limits the discharging current such that \[ I_{rd} = \frac{V_s}{R_1 + R_2} \]
The load can form a series circuit with the snubber network as shown in figure (e) below. The damping ratio of this second order system consisting RLC network is given as,

\[ \delta = \frac{\alpha}{\omega_0} = \frac{R_s + R}{2 \sqrt{\frac{C_s}{L_s + L}}} \],

where \( L_s \) stray inductance and \( L, R \) is load inductance and resistance respectively.

To limit the peak overshoot applied across the thyristor, the damping ratio should be in the range of 0.5 to 1. If the load inductance is high, \( R_s \) can be high and \( C_s \) can be small to retain the desired value of damping ratio. A high value of \( R_s \) will reduce discharge current and a low value of \( C_s \) reduces snubber loss. The damping ratio is calculated for a particular circuit \( R_s \) and \( C_s \) can be found.
Practical devices must be protected against high $\frac{di}{dt}$. As an example let us consider the circuit shown above, under steady state operation $D_m$ conducts when thyristor $T_i$ is off. If $T_i$ is fired when $D_m$ is still conducting $\frac{di}{dt}$ can be very high and limited only by the stray inductance of the circuit. In practice the $\frac{di}{dt}$ is limited by adding a series inductor $L_s$ as shown in the circuit above. Then the forward $\frac{di}{dt} = \frac{V_s}{L_s}$.

**Recommended questions:**

1. Distinguish between latching current and holding current.
2. Converter grade and inverter grade thyristors
3. Thyristor turn off and circuit turn off time
4. Peak repetitive forward blocking voltage $i^2t$ rating
5. Explain the turn on and turn of dynamic characteristics of thyristor
6. A string of series connected thyristors is to withstand a DC voltage of 12 KV. The maximum leakage current and recovery charge differences of a thyristors are 12 mA and 120 µC respectively. A derating factor of 20% is applied for the steady state and dynamic (transient) voltage sharing of the thyristors. If the maximum steady state voltage is 1000V, determine 1) the steady voltage sharing resistor $R$ for each thyristor. 2) the transient voltage capacitor $C_2$ for each thyristor
7. A SCR is to operate in a circuit where the supply voltage is 200 VDC. The $dv/dt$ should be limited to 100 V/µs. Series $R$ and $C$ are connected across the SCR for limiting $dv/dt$. The maximum discharge current from $C$ into the SCR, if and when it is turned ON is to be limited to 100 A. Using an approximate expression, obtain the values of $R$ and $C$. 

![Circuit Diagram](image-url)
8. With the circuit diagram and relevant waveforms, discuss the operation of synchronized UJT firing circuit for a full wave SCR semi converter.

9. Explain gate to cathode equivalent circuit and draw the gate characteristics. Mark the operating region.

10. Mention the different turn on methods employed for a SCR

11. A SCR is having a dv/dt rating of 200 V/µs and a di/dt rating of 100 A/µs. This SCR is used in an inverter circuit operating at 400 VDC and has 1.5Ω source resistance. Find the values of snubber circuit components.

12. Explain the following gate triggering circuits with the help of waveforms: 1) R – triggering 2) RC – triggering.