### Difference between Asynchronous and Synchronous Counter:

<table>
<thead>
<tr>
<th>Asynchronous Counter</th>
<th>Synchronous Counter</th>
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<tbody>
<tr>
<td>1. Clock input is applied to LSB FF. The output of first FF is connected as clock to next FF.</td>
<td>1. Clock input is common to all FF.</td>
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<td>2. All Flip-Flops are toggle FF.</td>
<td>2. Any FF can be used.</td>
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<tr>
<td>3. Speed depends on no. of FF used for n bit. [ f_{\text{max}} = \frac{1}{n \times t_p} ]</td>
<td>3. Speed is independent of no. of FF used. [ f_{\text{max}} = \frac{1}{t_p} ]</td>
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<tr>
<td>4. No extra Logic Gates are required.</td>
<td>4. Logic Gates are required based on design.</td>
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<tr>
<td>5. Cost is less.</td>
<td>5. Cost is more.</td>
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Unit 7: Sequential Design - I

Introduction, Mealy and Moore Models, State Machine Notation, Synchronous Sequential Circuit Analysis

Mealy and Moore Type Finite State Machines

There are two basic ways to design clocked sequential circuits. These are using:

1. Mealy Machine, which we have seen so far.


The objectives of this lesson are:

1. Study Mealy and Moore machines

2. Comparison of the two machine types

3. Timing diagram and state machines

Mealy Machine

In a Mealy machine, the outputs are a function of the present state and the value of the inputs as shown in Figure 1.

Accordingly, the outputs may change asynchronously in response to any change in the inputs.
Figure 1: Mealy Type Machine

Mealy Machine

In a Moore machine the outputs depend only on the present state as shown in Figure 2.

A combinational logic block maps the inputs and the current state into the necessary flip-flop inputs to store the appropriate next state just like Mealy machine.

However, the outputs are computed by a combinational logic block whose inputs are only the flip-flops state outputs.

The outputs change synchronously with the state transition triggered by the active clock edge.

Figure 2: Moore Type Machine

Comparison of the Two Machine Types

Consider a finite state machine that checks for a pattern of ‘10’ and asserts logic high when it is detected. The state diagram representations for the Mealy and Moore machines are shown in Figure 3.

The state diagram of the Mealy machine lists the inputs with their associated outputs on state transitions arcs.

The value stated on the arrows for Mealy machine is of the form Zi/Xi where Zi represents input value and Xi represents output value.